Remarks

Claims 2-11 and 13-28 have been amended. No new matter has been added.

Amendments to the Specification

The abstract is amended to comply with MPEP §608.01(b). Hence, Applicants respectfully request reconsideration of the specification in view of these amendments.

Claim Objections

Claims 2-11 and 13-28 were objected to for informalities. In response, these claims have been amended to provide sufficient antecedent basis. Thus, Applicants respectfully request reconsideration of these claims and withdrawal of the objections.

Claim Rejections Under 35 U.S.C. §102

Claims 1-30 stand rejected under 35 U.S.C. §102(a) as anticipated by Sheeran (*Checking safety properties using induction and a SAT-solver*, November 2000, In Proc. Conference on Formal Methods in Computer-Aided Design). Applicants respectfully traverse.

Independent claim 1 recites the following limitations:

(a) performing bounded verification on a circuit design for a number of transitions, the bounded verification corresponding to a predetermined limit for a number of transitions;

(b) performing induction proof of a first property for the number of transitions, wherein the induction proof is performed by a process comprising the acts of:

including, in an inductive set of one or more states, a plurality of states of the circuit design, wherein the inductive set of one or more states includes at least states passing the first property of the circuit design;

transitioning by at least one step, in a forward direction, states of the inductive set passing at least the first property of the circuit design, resulting in transitioned states;

determining if the transitioned states of the inductive set pass at least the first property of the circuit design;

repeating at least the transitioning and the determining, until at least, the determining results in the transitioned states of the inductive set passing or failing at least the first property of the circuit design; and

(c) if the at least one property is not verified, then increasing the limit for the bounded verification and repeating from (a).

Applicants respectfully submit that Sheeran does not disclose such limitations.

The Action purports that Sheeran discloses performing an induction based method of checking the property P by applying the induction depth to prove a property, wherein the number of transitions is limited to T, but can be extended by strengthened induction with depth "i", wherein "i" might be greater than zero and is a number of copies of T.

However, Sheeran specifically discloses, in page 110, that a sequence of "i" states define a path through T-transitions of "i", wherein a $path_i(s_0, s_i)$ indicates that there is a path from s_0 to s_i through "i" copies of T. In page 111, Sheeran discloses that a shortest path is loop-free and does not follow any repeat iterations. In page 116, Sheeran discloses that every loop-free path starting at an initial state (s_0) contains only P-states, and this concept is defined as strengthened induction with depth "i", wherein the term strengthened refers to the restriction to loop-free paths.

Accordingly, Sheeran does not disclose that, if induction proof of a property fails, then a limit for the bounded verification is increased, and the bounded verification and induction proof are repeated, in a manner as required by claim 1. In fact, Sheeran fails to disclose any increase in a limit of the bounded verification for any reason, much less an increase based failure to verify a property, in a manner as required by claim 1.

In Sheeran, the "i" variable is merely a variable that corresponds to a set of states $s_{[0..i]}$ that is checked using an SAT-solver to determine if the system is P-safe. The variable "i" is incremented to transition through the set of states. There is no disclosure in Sheeran that "i" is a limit of a bounded verification, much less that such a limit can be increased if there is a failure to verify a property.

In contrast, independent claim 1 of the present invention requires repeating at least the transitioning and the determining, until at least, the determining results in the transitioned states of the inductive set passing or failing at least the first property of the circuit design and, if the at least one property is not verified, then increasing the limit for the bounded verification and repeating the method from step (a).

For at least these reasons, it is respect fully submitted that claim 1, including claims dependent thereon, are allowable over the cited reference.

For at least the same reasons, it is respectfully submitted that independent claims 12 and 29, including claims dependent thereon, are also allowable over the cited reference.
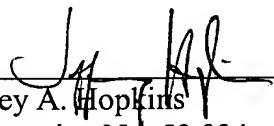
Conclusion

Based on the foregoing, all claims are believed allowable, and an allowance of the claims is respectfully requested. If the Examiner has any questions or comments, the Examiner is respectfully requested to contact the undersigned at the number listed below.

The Commissioner is authorized to charge any fees due in connection with the filing of this document to Bingham McCutchen's Deposit Account No. **50-2518,** referencing billing number **7038392001**. The Commissioner is authorized to credit any overpayment or to charge any underpayment to Bingham McCutchen's Deposit Account No. **50-2518,** referencing billing number **7038392001**.

Respectfully submitted,

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Date: August 24, 2006

By: _____

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